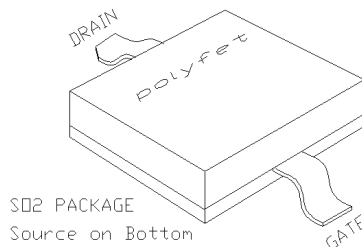




**General Description**

Silicon VDMOS and LDMOS transistors designed specifically for broadband RF applications. Suitable for Military Radios, Cellular and Paging Amplifier Base Stations, Broadcast FM/AM, MRI, Laser Driver and others.

"Polyfet"<sup>TM</sup> process features low feedback and output capacitances, resulting in high  $F_T$  transistors with high input impedance and high efficiency.



**SILICON GATE ENHANCEMENT MODE**

**RF POWER LDMOS TRANSISTOR**

**8.0 Watts Single Ended**

**Package Style S02**

**HIGH EFFICIENCY, LINEAR**

**HIGH GAIN, LOW NOISE**

**ROHS COMPLIANT**

**ABSOLUTE MAXIMUM RATINGS ( T = 25 °C )**

Total Device Dissipation	Junction to Case Thermal Resistance	Maximum Junction Temperature	Storage Temperature	DC Drain Current	Drain to Gate Voltage	Drain to Source Voltage	Gate to Source Voltage
50 Watts	3.40 °C/W	200 °C	-65 °C to 150 °C	5.0 A	36 V	36 V	20 V

**RF CHARACTERISTICS ( 8.0 WATTS OUTPUT )**

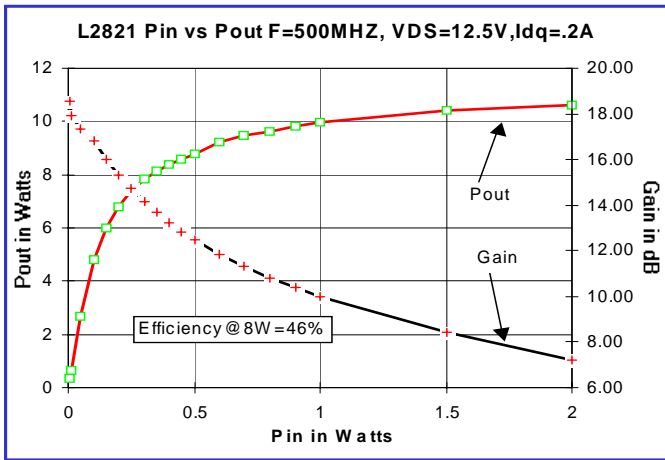
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Gps	Common Source Power Gain	13			dB	Idq = 0.20 A, Vds = 12.5 V, F = 500 MHz
$\eta$	Drain Efficiency		50		%	Idq = 0.20 A, Vds = 12.5 V, F = 500 MHz
VSWR	Load Mismatch Tolerance			20:1	Relative	Idq = 0.20 A, Vds = 12.5 V, F = 500 MHz

**ELECTRICAL CHARACTERISTICS ( EACH SIDE )**

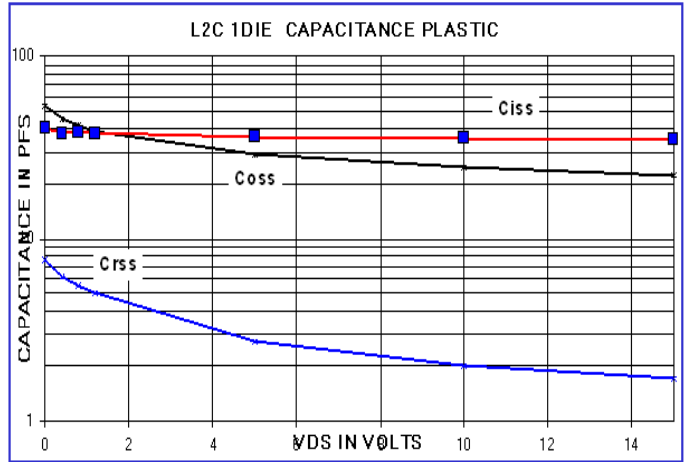
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Bvdss	Drain Breakdown Voltage	36			V	Ids = 0.10 mA, Vgs = 0V
Idss	Zero Bias Drain Current			1.0	mA	Vds = 12.5 V, Vgs = 0V
Igss	Gate Leakage Current			1	uA	Vds = 0V Vgs = 30V
Vgs	Gate Bias for Drain Current	2		5	V	Ids = 0.10 A, Vgs = Vds
gM	Forward Transconductance		1.0		Mho	Vds = 10V, Vgs = 5V
Rdson	Saturation Resistance		0.60		Ohm	Vgs = 20V, Ids = 3.00 A
Idsat	Saturation Current		7.50		Amp	Vgs = 20V, Vds = 10V
Ciss	Common Source Input Capacitance		33.0		pF	Vds = 12.5 Vgs = 0V, F = 1 MHz
Crss	Common Source Feedback Capacitance		2.0		pF	Vds = 12.5 Vgs = 0V, F = 1 MHz
Coss	Common Source Output Capacitance		24.0		pF	Vds = 12.5 Vgs = 0V, F = 1 MHz

# L2821

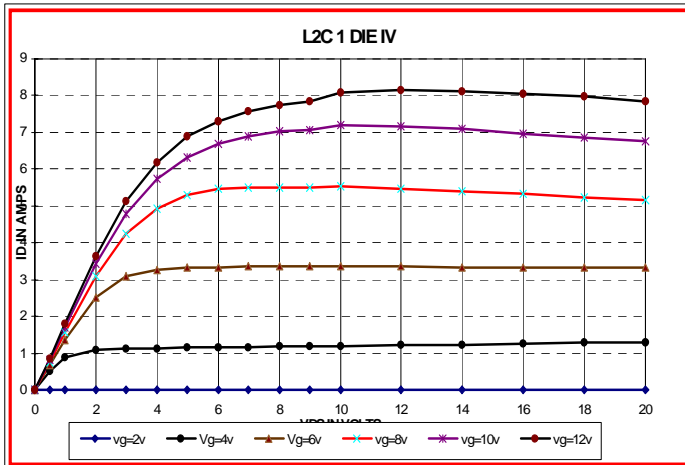
POUT VS PIN GRAPH



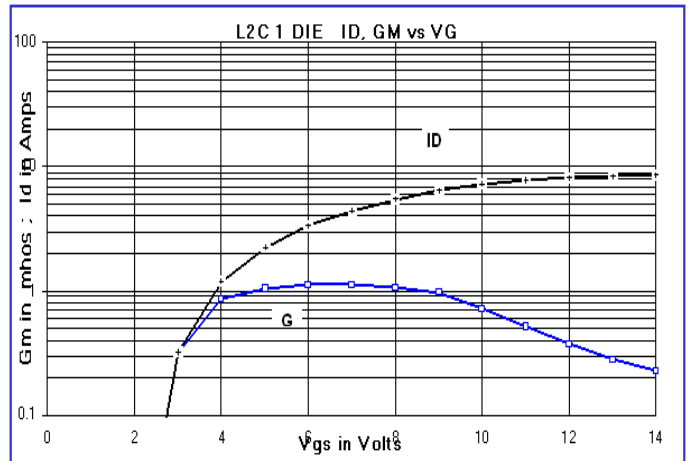
CAPACITANCE VS VOLTAGE



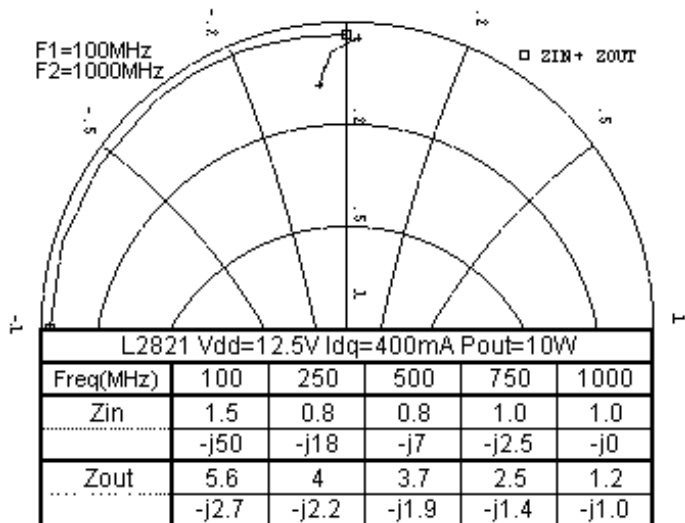
IV CURVE



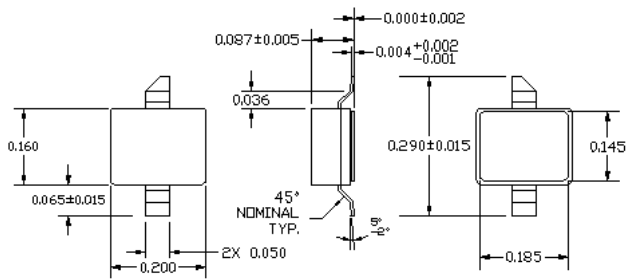
ID & GM VS VGS



Zin Zout



PACKAGE DIMENSIONS IN INCHES



POLYFET S02 PACKAGE

Tolerance .XX +/-0.01 .XXX +/-0.005 inches