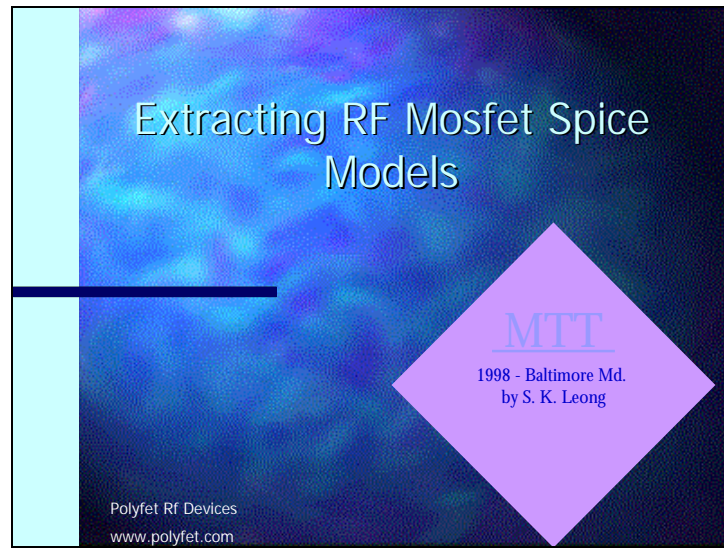
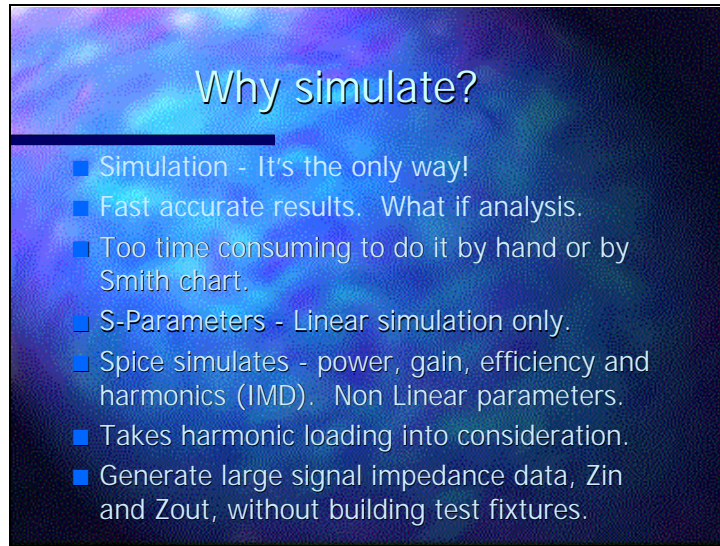


Slide 1



This presentation is available on our web site



Why simulate?

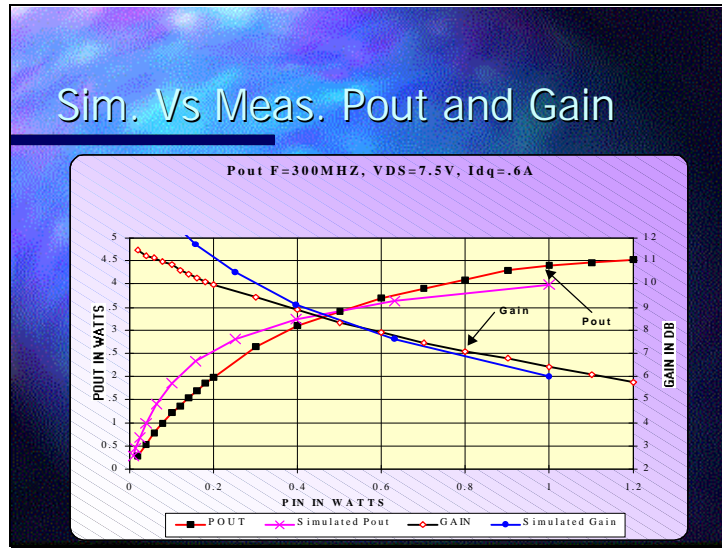
- Simulation - It's the only way!
- Fast accurate results. What if analysis.
- Too time consuming to do it by hand or by Smith chart.
- S-Parameters - Linear simulation only.
- Spice simulates - power, gain, efficiency and harmonics (IMD). Non Linear parameters.
- Takes harmonic loading into consideration.
- Generate large signal impedance data, Z_{in} and Z_{out} , without building test fixtures.

With today's simulation tools available, high power rf design does not have to be a tedious task anymore. The days of trial and error are passe and soon too will be manual graphing on the Smith Chart.

Unlike linear designs using S parameters, the lack of good high power transistor models has hampered the industry from using simulation for non-linear designs. Polyfet RF Devices supplies Spice Models for all their transistors. For other manufacturers, it might be necessary to extract models for your own use.

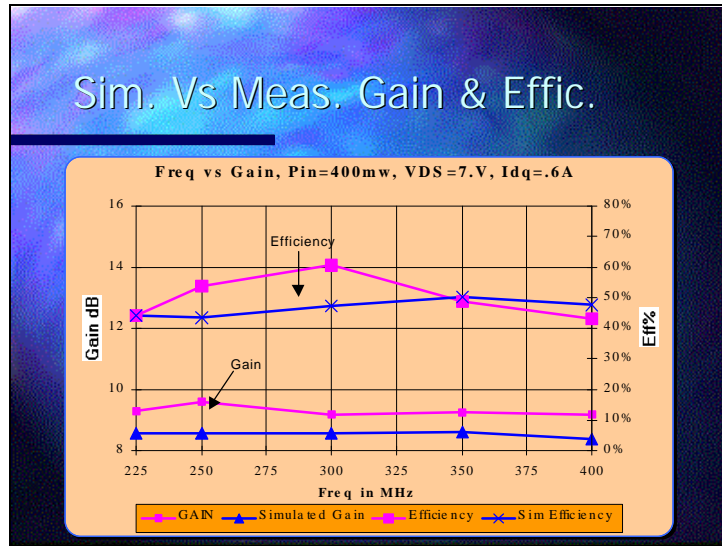
The following graphs show simulation vs. actual measured results demonstrating the usefulness of simulation. Unlike using S parameters or Z_{in} Z_{out} , using Spice provides the advantage of analyzing non-linear behavior and efficiency. With today's requirements in designing for digital radios linearity and efficiency are critical parameters and simulation using Spice enable accurate results.

Slide 3



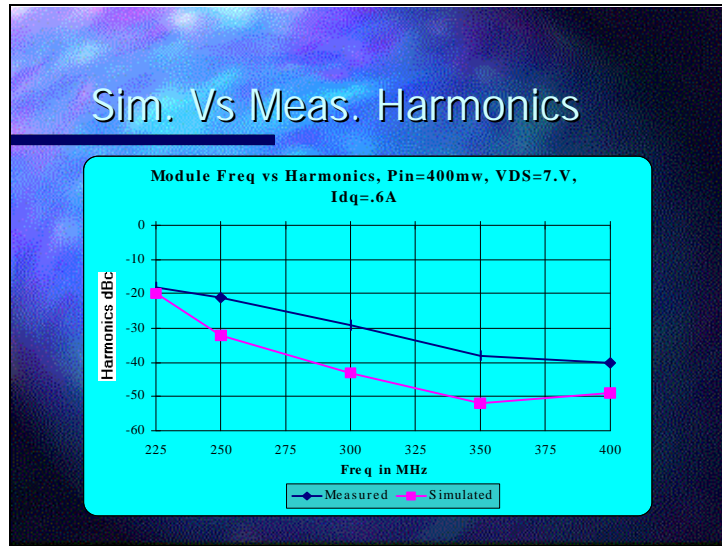
Demonstration of Accuracy in simulating Power output and gain of amplifier.

Slide 4

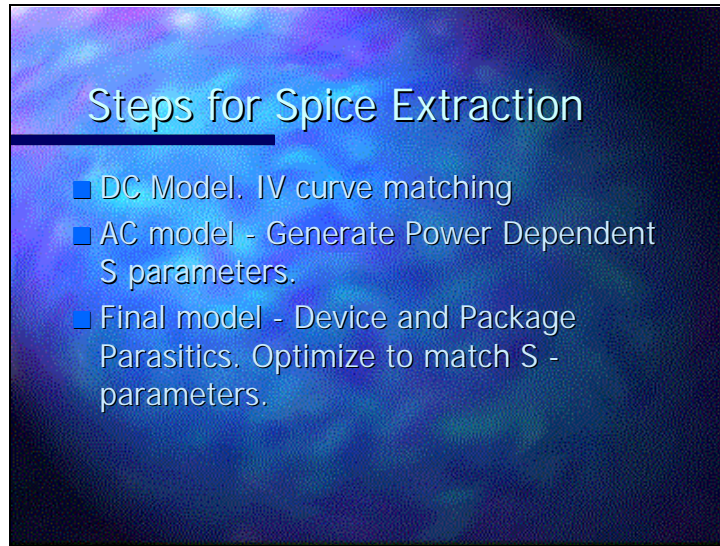


Demonstration of accuracy in simulating gain and efficiency over a broad bandwidth.

Slide 5



Demonstration of simulation of 2nd Harmonic



Procedures to extract Spice models

Reference Books:-

Semiconductor Device Modeling - Palo Antognetti and Giuseppe Massobrio

Spice-Practical Device Modeling - Ron Kielkowski

“Spicing-up SPICE II Software for Power Mosfet Modeling” Dolny et el. RCA Application Note AN-8160

“Device Modeling High Power DMOS Transistor Amplifiers” Steve Hamilton and Octavius Pitzalis Jr. EEsof Application Note.

Need to measure DC characteristics, capacitances and S parameters in order to generate Spice models

DC Model

- Good to know Gate Length (channel length) and Gate Width (Perimeter)
- Measure IV curves.
- Curve fit model to IV data.
- Mosfet in series with Jfet.
- Spice - Berkeley 2G.6 Level 1.

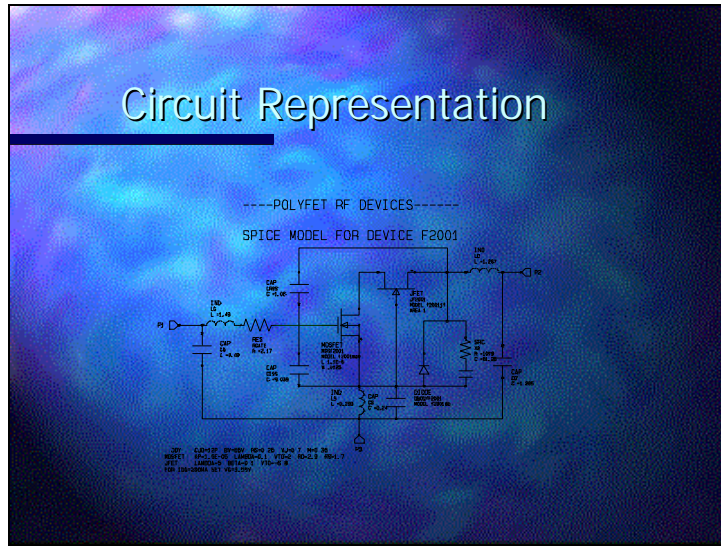
VGS (Volts)	ID (µA) at VGS=0	ID (µA) at VGS=2	ID (µA) at VGS=4	ID (µA) at VGS=6	ID (µA) at VGS=8	ID (µA) at VGS=10
0	0	0	0	0	0	0
2	0	0.5	1.5	2.5	3.5	4.5
4	0	1.5	2.5	3.5	4.5	5.5
6	0	2.5	3.5	4.5	5.5	6.0
8	0	3.5	4.5	5.5	6.0	6.5
10	0	4.5	5.5	6.0	6.5	7.0
12	0	5.5	6.0	6.5	7.0	7.5
14	0	6.0	6.5	7.0	7.5	8.0
16	0	6.5	7.0	7.5	8.0	8.5
18	0	7.0	7.5	8.0	8.5	9.0
20	0	7.5	8.0	8.5	9.0	9.5

Device design information is needed from Manufacturer. - gate length and gate Width. If not, set $L/W=1$ and adjust K_p to fit.

Use Curve tracer or equivalent to measure I-V curves.

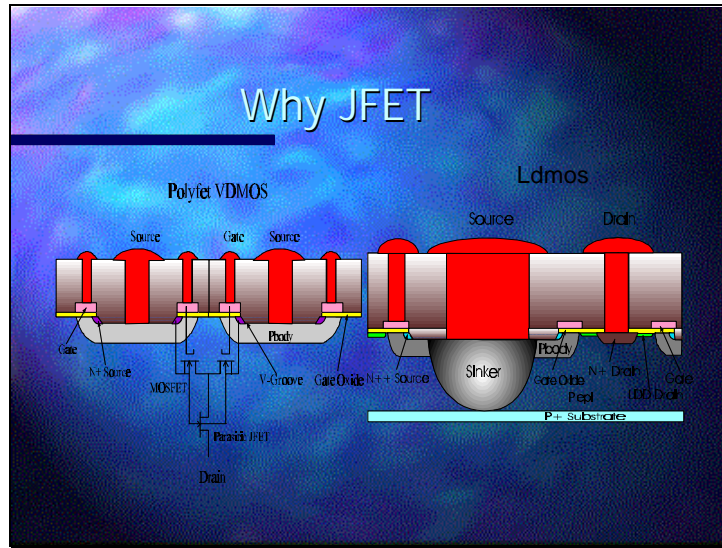
Curve fit IV plot.

V_t , K_p can be extracted by measuring I_d Vs V_{gs} .

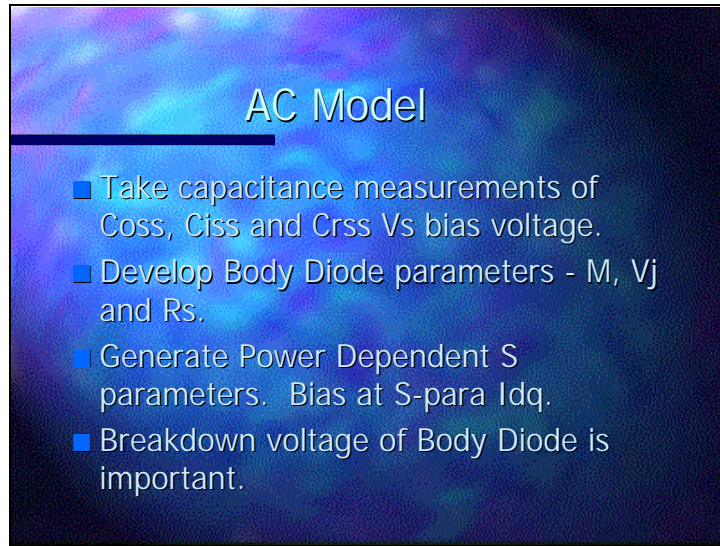


Schematic representation of Spice Model showing Mosfet and Jfet.

Applies to both VDMOS and LDMOS.



Cross section view of VDMOS showing parasitic Jfet in the vertical drain region. LDMOS has a horizontal drain drift region which is modeled by using the Jfet.

A slide titled "AC Model" with a blue and purple background. The title is centered at the top. Below the title is a horizontal line. Underneath the line is a bulleted list of four items, each starting with a blue square bullet point.

AC Model

- Take capacitance measurements of C_{oss} , C_{iss} and C_{rss} Vs bias voltage.
- Develop Body Diode parameters - M , V_j and R_s .
- Generate Power Dependent S parameters. Bias at S-para I_{dq} .
- Breakdown voltage of Body Diode is important.

Measure the 3 parasitic capacitances. Use the C_{oss} curve Vs bias voltage to obtain V_j and m for the body diode.

Set bias current at the current level used to measure S parameters. Generate Power Dependent S parameters. Body Diode BV setting is important.

Power Dependent S parameter is generated from the 3 active elements - MOSFET, JFET and DBODY



Validate and Verify

- Simulate and build amp.
- Watch out for optimizer limitations.
- Watch out for harmonics loading.
- Practice and build on experience.

It is not expected to have the simulated data and the built up amplifier to be identical. Since transistors vary from lot to lot, fine tuning at the amplifier level is expected. The values of inductance and capacitance can vary from simulation to final can be off as much as 25%. However, without simulation, we wouldn't even be this close. Often manual tuning is required as Optimizer has limitations. It is also found useful to simulate Z_{in} Z_{out} values and use those as loads to optimize the matching network, rather than letting the Optimizer match the matching network to the transistor.