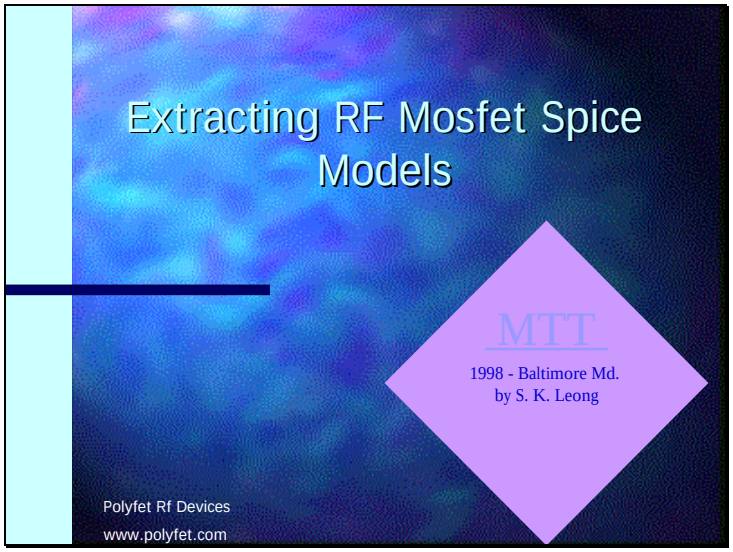
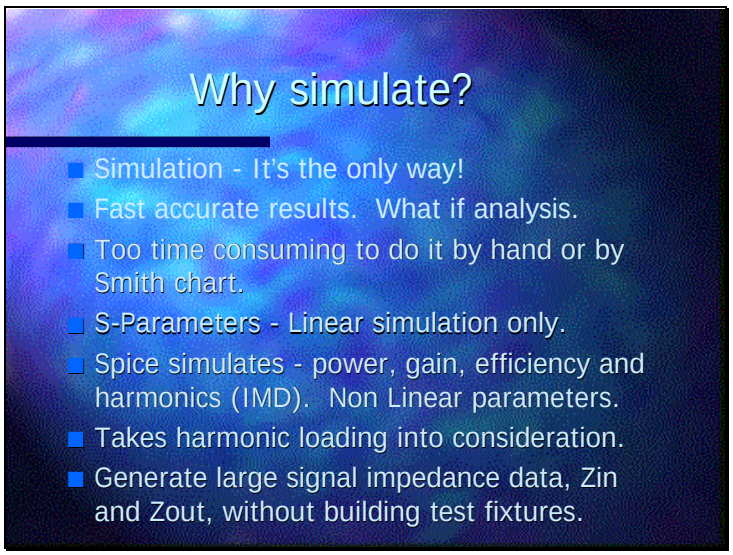
Slide 1



This presentation is available on our web site

Slide 2

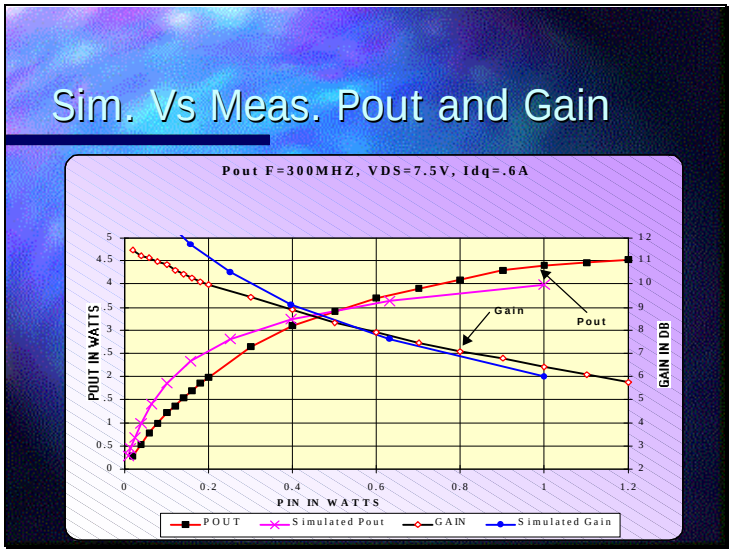


With today's simulation tools available, high power rf design does not have to be a tedious task anymore. The days of trail and error are passe and soon too will be manual graphing on the Smith Chart.

Unlike linear designs using S parameters, the lack of good high power transistor models has hampered the industry from using simulation for non-linear designs. Polyfet RF Devices supplies Spice Models for all their transistors. For other manufacturers, it might be necessary to extract models for your own use.

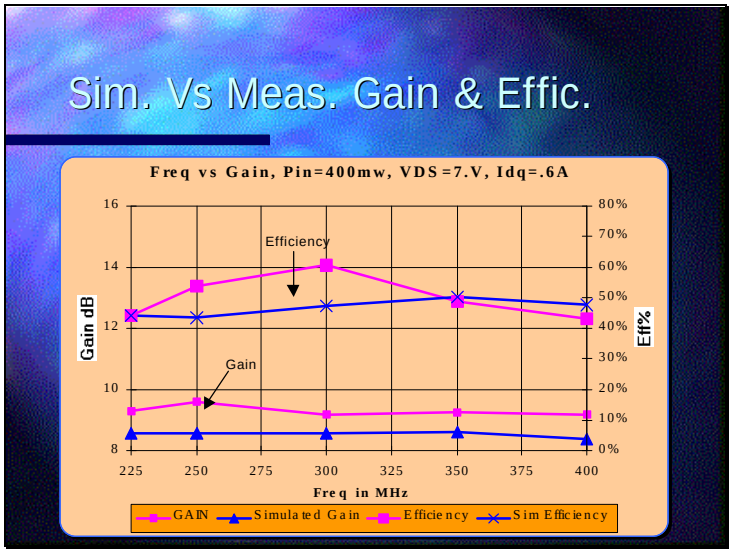
The following graphs show simulation vs. actual measured results demonstrating the usefulness of simulation. Unlike using S parameters or Zin Zout, using Spice provides the advantage of analyzing non-linear behavior and efficiency. With today's requirements in designing for digital radios linearity and efficiency are critical parameters and simulation using Spice enable accurate results.

Slide 3



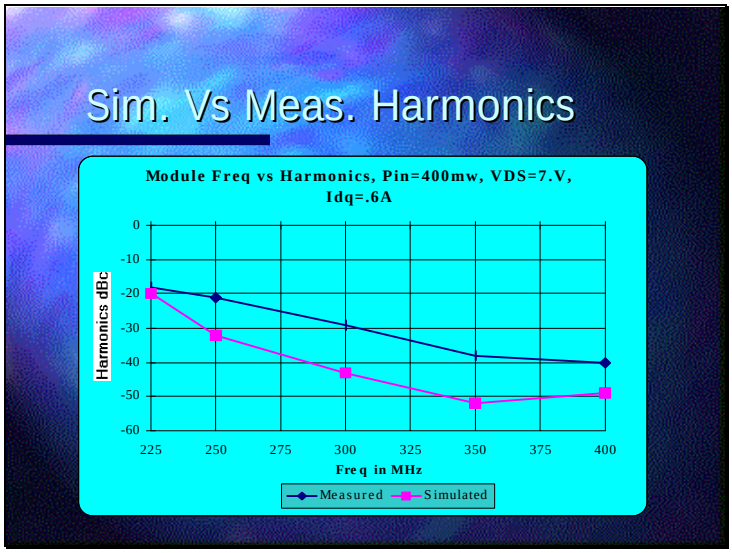
Demonstration of Accuracy in simulating Power output and gain of amplifier.

Slide 4



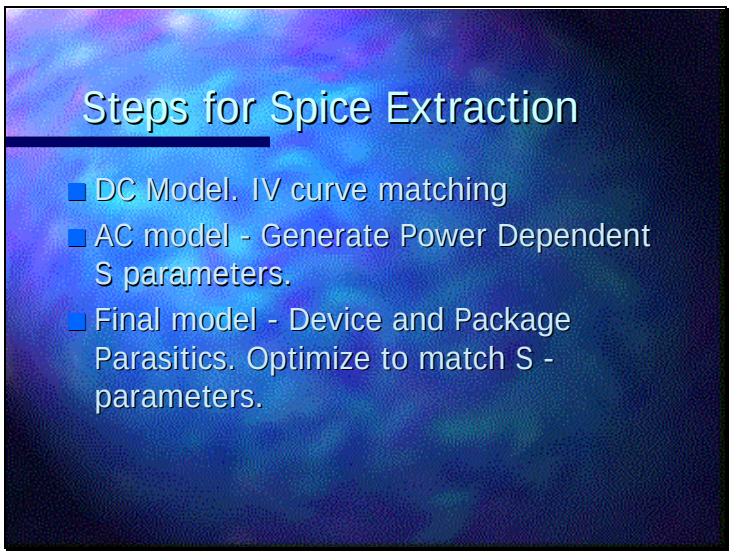
Demonstration of accuracy in simulating gain and efficiency over a broad bandwidth.

Slide 5



Demonstration of simulation of 2nd Harmonic

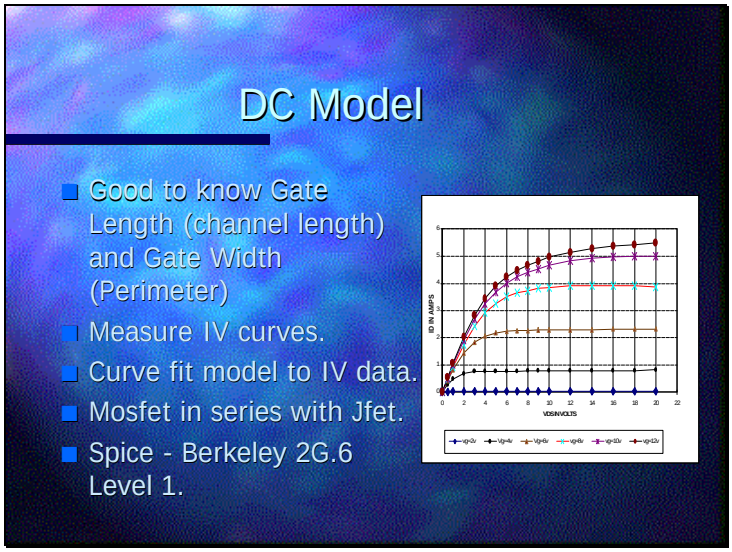
Slide 6



<u>Procedures to extract Spice models</u>
Reference Books:-
Semiconductor Device Modeling - Palo Antognetti and Giuseppe Massobrio
Spice-Practical Device Modeling - Ron Kielkowski
“Spicing-up SPICE II Software for Power Mosfet Modeling” Dolny et el. RCA Application Note AN-8160
“Device Modeling High Power DMOS Transistor Amplifiers” Steve Hamilton and Octavius Pitzalis Jr. EEsof Application Note.

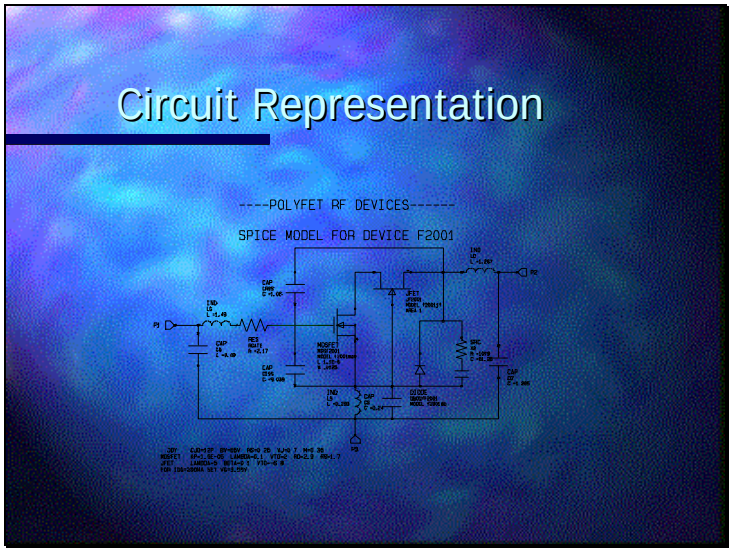
Need to measure DC characteristics, capacitances and S parameters in order to generate Spice models

Slide 7



Device design information is needed from Manufacturer. - gate length and gate Width. If not, set L/W=1 and adjust Kp to fit.
Use Curve tracer or equivalent to measure I-V curves.
Curve fit IV plot.
Vt, Kp can be extracted by measuring Id Vs Vgs.

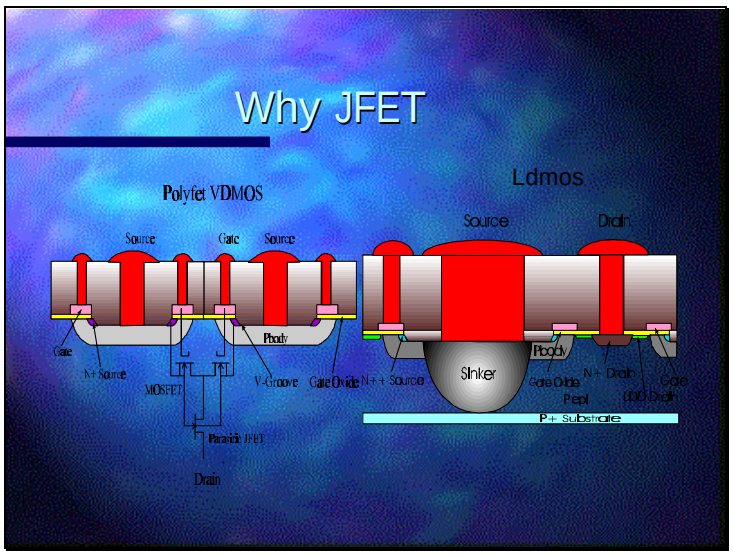
Slide 8



Schematic representation of Spice Model showing Mosfet and Jfet.

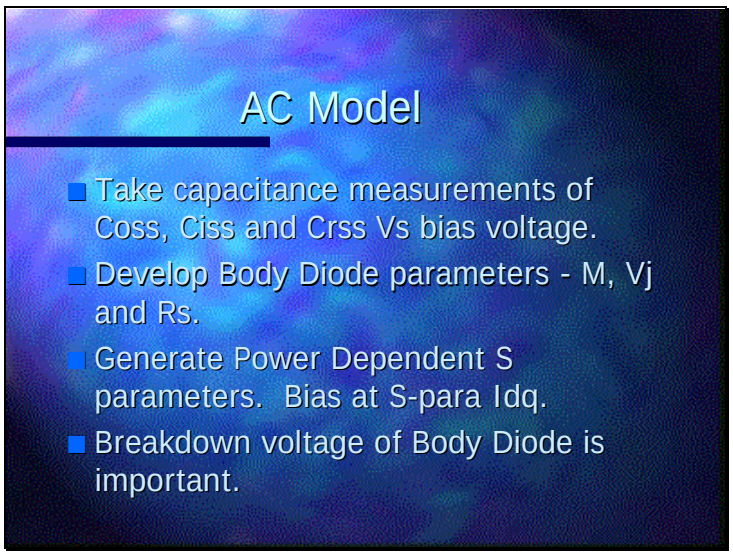
Applies to both VDMOS and LDMOS.

Slide 9



Cross section view of VDMOS showing parasitic Jfet in the vertical drain region. LDMOS has a horizontal drain drift region which is modeled by using the Jfet.

Slide 10

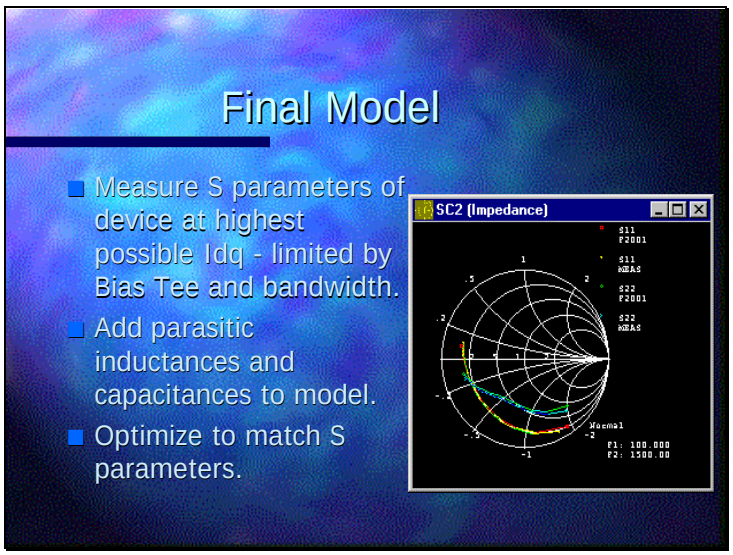


Measure the 3 parasitic capacitances. Use the Coss curve Vs bias voltage to obtain Vj and m for the body diode.

Set bias current at the current level used to measure S parameters. Generate Power Dependent S parameters. Body Diode BV setting is important.

Power Dependent S parameter is generated from the 3 active elements - MOSFET, JFET and DBODY

Slide 11



Finalize the Spice model with package capacitances.
A linear simulator is used to match measured data to simulated data. Simulation programs with optimization capability is necessary in order to perform this operation. Using the optimizer, parasitic capacitances and inductances are varied so simulated S-parameter best match measured S-parameters data.

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It is not expected to have the simulated data and the built up amplifier to be identical. Since transistors vary from lot to lot, fine tuning at the amplifier level is expected. The values of inductance and capacitance can vary from simulation to final can be off as much as 25%. However, without simulation, we wouldn't even be this close.
Often manual tuning is required as Optimizer has limitations. It is also found useful to simulate Zin Zout values and use those as loads to optimize the matching network, rather than letting the Optimizer match the matching network to the transistor.